A SPICE Compatible Macromodel for CMOS Operational Amplifiers

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Abstract

A SPICE macromodel that captures the "personality" of National Semiconductor's CMOS op-amps has been developed. The salient features of the macromodel are a MOSFET input stage, Miller compensation, and a current-source output stage. A description of the model will be given along with correlation to actual device behavior.

Introduction

Recently, there has been a major thrust in lowering power dissipation and supply voltages for analog system level design. In response to this, National Semiconductor has developed a family of CMOS op-amps which feature rail-to-rail output swing, extremely low input bias current (10 fA typ.), single supply operation, low power consumption, and an input common-mode range that includes the negative supply rail [1]. Due to the unique topology that makes these features possible, a new SPICE macromodel was required in order to achieve accurate simulation results.

Macromodeling Philosophy

The philosophy used in creating this macromodel was a desire to design a model that would accurately simulate the typical behavior of a CMOS op-amp while executing much faster than a device level model (commonly referred to as a micromodel). The "personality" of an op-amp can be captured by individually hand crafting and thoroughly testing each model to ensure that it accurately simulates the behavior of the real device.

CMOS Macromodel Input Stage

The input stage performs several important functions including non-linear input transfer characteristics, offset voltage, input bias currents, second pole, and quiescent power supply current. The heart of the input stage consists of a differential amplifier which is made up of two simplified MOSFET models (see *Figure 1*) [2]. Input common-mode range can be modeled by properly setting the zero bias threshold voltage (V_{TO}) in the MOSFET model. In the case of the LMC6484, which has rail-to-rail input common-mode range, V_{TO} is left at its default value of zero. Offset voltage is modeled with an ideal voltage source, E_{OS}, while input bias/offset currents are modeled by properly setting the leakage currents on the input protection diodes DP1–DP4. Quiescent current is modeled with the combination of I2 and the R8–R9 series resistors. As the supply voltage increases, the current through R8 and R9 will increase, effectively simulating that behavior in the real device. Resistors R8 and R9 also act as a voltage divider and establish a common-mode voltage (V_H) for the model directly between the rails. If the supply rails are symmetrical, i.e. ±5V, node 49 will be at 0V. Voltage-controlled voltage-source, EH, measures the voltage across R8 and subtracts an equal voltage from the positive supply rail to provide a stiff point between the rails (node 98) to which many other stages in the model are referenced. Voltage-controlled current-source G0 and resistor R0 model the gain of the input stage. The signal is then passed to the frequency shaping stages for further conditioning.

Frequency Shaping Stages

In keeping with the philosophy of providing a macromodel that is as accurate as possible, it has been determined that the model must be capable of easily accommodating as many poles and zeros that are necessary to precisely shape the magnitude and phase response of the model [3]. This is accomplished with telescopic frequency shaping stages that each have unity DC gain, making it easier to add poles and zeros without changing the low-frequency gain of the model. Each of the three types of frequency-shaping stages is shown in *Figure 1*.

Common-Mode Stage

Common-mode gain is modeled with a common-mode zero stage whose gain increases as a function of frequency. A voltage-controlled current-source, G4, is controlled with a polynomial equation which adds the voltage at each input (nodes 1 and 2) and divides the sum by two. This result is the input common-mode voltage. The DC gain of the stage is set to the reciprocal of the CMRR for the amplifier. An inductor, L2, increases the gain of the stage at 20 dB/decade to model the roll-off of CMRR that occurs in most amplifiers. The output of the common-mode zero stage (node 16) is reflected to the E_{OS} source to provide an input-referred common-mode error.

Characteristics of National Semiconductor's CMOS Operational Amplifiers

Common Characteristics	Rail-to-rail output swing, ultra-low input bias current (10 fA typ.), low drift (1.3 µV/°C), single supply operation, input common-mode range includes ground, low power consumption, and high voltage gain.
LMC660	Drives 600Ω load, high bandwidth (1.4 MHz), high slew rate (1.1 V/µs), comes in quad and dual (LMC662).
LPC660	Low power (215 µW/amp), comes in quad and dual (LPC662).
LMC6044	Low power (70 µW/amp), comes in quad, single (LMC6041) and dual (LMC6042).
LMC6062	High precision dual (V_{OS} = 100 µV), low power (80 µW/amp).
LMC6082	High precision dual (V_{OS} = 150 µV), drives 600Ω loads, high bandwidth (1.3 MHz).

Common-Mode Stage (Continued)

Characteristics of National Semiconductor's CMOS Operational Amplifiers (Continued)

LMC6484	Rail-to-rail input common-mode range, operates on 3V single supply, drives 600Ω loads, high bandwidth (1.3 MHz), comes in quad and dual (LMC6482).

National's CMOS Op-Amp Macromodel

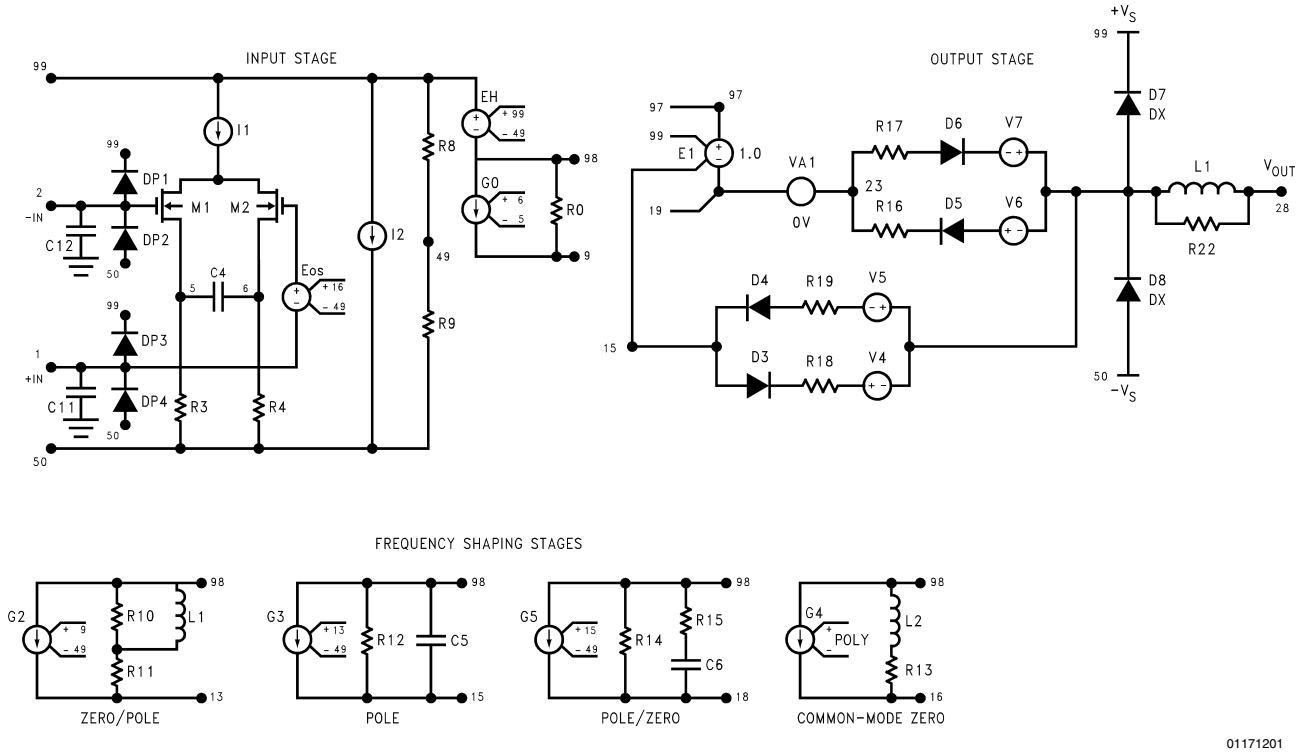


FIGURE 1.

Output Stage

After the last frequency-shaping stage, the intermediate signal is sent to the output stage. The output stage performs several important functions including dominant pole, slew rate limiting, dynamic supply current, short-circuit current limiting, the balance of the open-loop gain, output swing limiting, and output impedance. The output stage of the macromodel incorporates several new innovations in order to accommodate the unique topology of National's CMOS op-amps. To understand the unique features of this topology, a description of the actual amplifier output stage is in order.

The main feature of National's CMOS amplifiers is that the output can swing rail-to-rail. This is accomplished by removing the traditional output buffer and taking the output directly from the integrator. The output portion of the integrator is a common-source complementary push-pull gain stage which functions as a current source. Depending on load resistance, the output stage can have a considerable amount of gain. However, since the internal compensation capacitor is referenced to the output node, the slew rate does not significantly change as the output is loaded. Also, loading the output will reduce the open-loop gain of the amplifier so that the first pole will increase in frequency in order to maintain the gain-bandwidth product of the amplifier.

In the model, Miller compensation was used to obtain an additional degree of freedom in setting the open-loop gain, slew rate, and first pole. The slew rate is defined by:

$$SR = \frac{I1}{C3}$$

while the first pole is determined with the equation:

$$f_{p1} = \frac{1}{2 \times \pi \times R5 \times C3 \times (1 + A_{VOUT})}$$

where A_{VOUT} is the gain of the output stage. Note that the slew rate can be set with C3 while the first pole can be independently set with the gain of the output stage. A gain stage consisting of a voltage-controlled current-source G1 and resistor R5 takes the signal from the last frequency-shaping stage and amplifies it by the balance of the open-loop gain ($G1 \times R5 = A_{VOL} - A_{VIN} - A_{VOUT}$). A voltage clamp made of D1, V2, D2, and V3 limits the drive to the output current-source, G6, to provide short-circuit current limiting. Since the output stage has gain, output swing limit-

Output Stage (Continued)

ing is performed at the output node with a clamp consisting of D5, V4, D6, and V5. A resistor, R17, models the slight degradation in output swing as the amplifier is loaded.

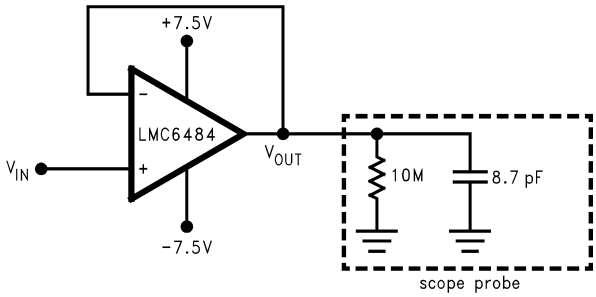
Dynamic Supply Current

A behavior that is often not included in op-amp macromodels is dynamic supply current. If the output of the model is an ideal current source, the simulated output current of the model appears to come from nowhere, i.e., the supply currents do not change. This apparent violation of the second law of thermodynamics has been solved with diodes D7–D8, current sources F5–F6, and associated circuitry. Since it is important to keep non-linear devices, such as diodes, out of the signal path, only an ideal ammeter, VA8, was inserted in the output driver to sense the sinking or sourcing of output current. Current-controlled current-source, F5, mirrors the current sensed by VA8 and forces an equal current through either D7 or D8 depending on its polarity. If current is being sourced into the load, the current flows from the positive rail through E1, VA8, and G6 to the output node and no supply current correction is necessary. However, if the output stage is sinking current from the load, the current flows from the output node up through G6, VA8 and E1 into the positive rail. To compensate for this, F5 forces an equal current through D7 and ammeter VA7. This current is then mirrored to current-source F6 which pulls an equal amount of current out of the positive rail and forces it into the negative rail. Therefore, if the output stage is sourcing current, it appears to come from the positive rail, whereas current that is sinking from the load appears to go into the negative rail. The net result of all these extra devices is an output stage which closely models the behavior of the real amplifier.

Simulation Accuracy

To ensure the accuracy of the macromodel, the simulation results are compared to lab data taken from an actual device. *Figure 2* shows a typical voltage follower transient response test circuit and *Figure 3* shows a SPICE netlist [4] for simulating the small-signal transient response of the LMC6484. Notice that the simulated response shown in *Figure 5* compares quite closely with the actual response shown in *Figure 4* with the correct amount of over-shoot and frequency of ringing.

Figures 6, 7 demonstrate the rail-to-rail input and ouput capabilities of the actual LMC6484 and the model respectively. The amplifier was configured as a voltage follower and powered from a 3V single supply. Then, a 3 V_{PP} square-wave was applied to the non-inverting input. The amplifier is clearly capable of handling this rail-to-rail input and reproducing it on the output while driving a 4.7 kΩ load. The simulation results show that the macromodel accurately models the slew rate and output swing of the amplifier.



Note: It is very important to include a model of the scope probe on the output of the amplifier to obtain reasonable results from the simulation.

FIGURE 2. Non-Inverting Amplifier (A_V = +1)

```
* LMC6484 S.S. Pulse Response. V(6)
* Cload = scope
*
XAR1 3 6 7 4 6 LMC6484
VP 7 0 7.5V
VN 4 0 –7.5V
VIN 3 0 PULSE (–.1V .1V 3U 20N 20N 5U)
Rout 6 0 10MEGohm
Cout 6 0 8.7pF
.LIB CMOSOA.LIB
.TRAN/OP .1N 10U
.PROBE
.END
```

FIGURE 3. Non-Inverting Amplifier Netlist to Simulate the Small-Signal Response of the LMC6484 [4]

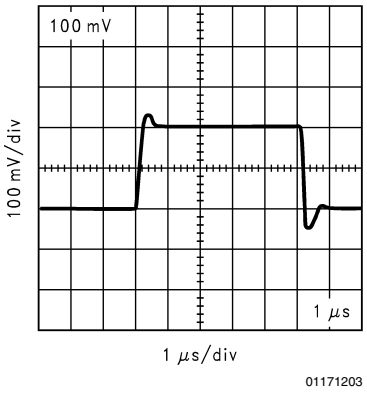


FIGURE 4. LMC6484 Small-Signal Transient Response

Simulation Accuracy (Continued)

LMC6484 S.S. Pulse Response (V(6) C_{LOAD} = scope)

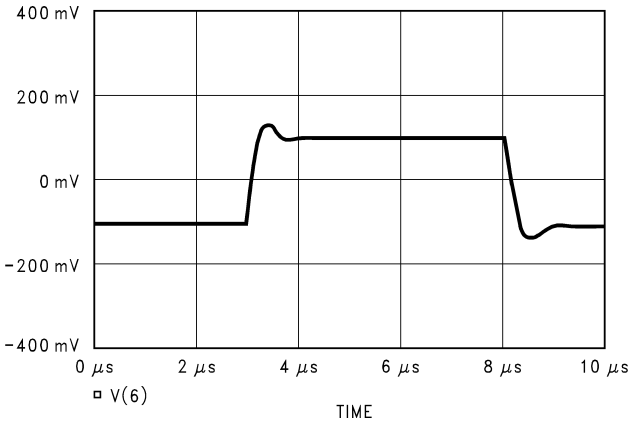
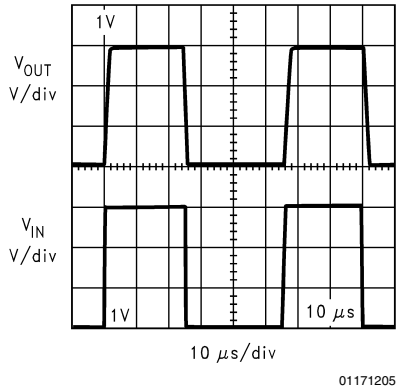


FIGURE 5. Simulated Small-Signal Transient Response



Note: This image demonstrates the rail-to-rail input/output capabilities of the LMC6484 while powered from a 3V single supply and driving a 4.7 kΩ load. Don't try this with an ordinary op-amp.

FIGURE 6. Large-Signal Transient Response

LMC6484 L.S. Pulse Response
(A_V = +1, V_{SUPP} = 0, +3, R1 = 4.7k)

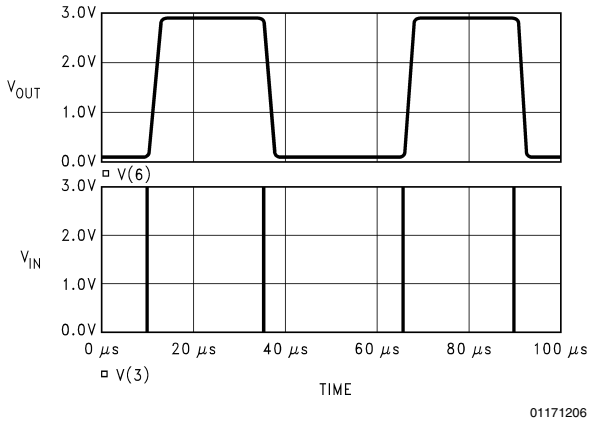


FIGURE 7. LMC6484 Simulated Large-Signal Transient Response

Conclusion

An accurate SPICE macromodel has been developed that captures the "personality" of National Semiconductor's CMOS operational amplifiers. The macromodel includes effects such as rail-to-rail output swing, input common-mode range, MOSFET input stage transfer characteristics, accurate frequency and transient response, slew rate and output short-circuit current. The model is not capable of simulating PSRR, thermal effects, or noise at this time.

Since the macromodels are much less complex and have fewer p-n junctions than a transistor level micromodel, simulation speed is much faster. For example, an LMC6484 macromodel simulation executed 34 times faster than its transistor level model. With accurate macromodels, the designer can quickly determine the dominant effects of a circuit and explore effects that are difficult to obtain with lab bench evaluation.

References

1. Monticelli, D.M.: "A Quad CMOS Single-Supply Op Amp with Rail-to-Rail Output Swing", *IEEE Journal of Solid State Circuits,* Dec. 1986 Vol. SC-21.
2. Boyle, G.R.: "Macromodeling of Integrated Circuit Operational Amplifiers", *IEEE Journal of Solid-State Circuits,* Dec. 1974 Vol. SC-9.
3. Alexander, Mark: *AN-138 Spice-Compatible Op Amp Macromodels,* Precision Monolithics Inc., Application Note 138.
4. Tuinenga, Paul: *SPICE: A Guide to Circuit Simulation & Analysis Using PSpice®*, Prentice-Hall, 1992.

Notes

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