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Microchip's Op Amp SPICE Macro Models

Author: *Yang Zhen*
(Microchip Technology Inc.)
Ron Wunderlich
(Innovative Ideas and Design)

INTRODUCTION

The SPICE macro models for Microchip's operational amplifiers (op amps) aid in the design and analysis of various circuits by allowing for detailed simulation of the circuit being designed.

This application note covers the function and use of Microchip's op amp SPICE macro models. It does not explain how to use the circuit simulator but will give the user a better understanding how the model behaves and tips on convergence issues.

MODEL DESCRIPTION

Microchip's op amp SPICE macro models were written and tested in Orcad's PSPICE 10.0 which is equivalent to Cadence PSPICE 15.x. The type of modeling technique that was used to model the op amps is called "Macro Modeling". It is based on treating the op amp as a black box and using mathematical equivalents of the internal functions. As opposed to macro modeling, transistor level modeling is used for modeling of the device under development and fabrication.

There are many advantages of macro modeling over transistor level modeling. Since the op amp internal circuitry has been simplified to mathematically represent the functions, the simulation runs much faster and is more robust. This allows the user to simulate their circuitry at the board or system level with the op amps within a reasonable simulation time. Since the model is more robust, it allows flexibility in the convergence criteria so that it can more easily work with more types of circuits.

However, with transistor level modeling, there are many interactions between the transistors such as the variations of voltage and current with time or temperature. In a macro model, some of these variations have to be simplified. For example, the quiescent current will vary smoothly over temperature for an actual IC or transistor level model. To model this using the macro modeling technique, a look-up table is used. This causes the macro model results to not be as smooth as the actual IC. However the discrepancies between the look-up table and the actual IC performance are minimal.

What The Models Cover

Microchip's op amp SPICE macro models cover a wide aspect of the op amp's electrical specifications. Not only do the models cover voltage, current, and resistance of the op amp, but it also covers the temperature and noise effects on the behavior of the op amp.

The models have been verified by comparing simulation results against actual op amp specifications contained in the appropriate op amp data sheet.

The op amp SPICE macro models have not been verified outside of the specification range listed in the op amp data sheet. The model behaviors under these conditions cannot be guaranteed that it will match the actual op amp performance.

Some of the op amps with high output impedance could not be easily modeled to operate in both linear applications and in comparator applications. For these op amps, it was decided that two op amp models be developed. One operates normally as an op amp in linear applications and the other one as a comparator. The comparator models are denoted with the word "COMP" after the name of the model. For example, the model MCP6031 should be used for op amp in linear applications and another model MCP6031COMP should be used for comparator applications.

Using The Op Amp SPICE Macro Models

Microchip's op amp SPICE macro models are provided in netlist format. This is useful for simulating the models in a number of different simulators. Please refer to your simulator software reference manual on how to create a schematic symbol and relating a netlist to the symbol. All SPICE simulation schematic tools are different in their creation of a schematic symbol and relating it to the library file.

The op amp model is in sub circuit format. An example of this sub-circuit can be found in Figure 1.

```
.SUBCKT MCP6241  1 2 3 4 5
*                | | | | |
*                | | | | Output
*                | | | Negative Supply
*                | | Positive Supply
*                | Inverting Input
*                Non-inverting input
.
... (Rest of MCP6241 Netlist)
.ENDS MCP6241
```

FIGURE 1: *MCP6241 Sub Circuit.*

This model has five nodes: Non-inverting Input, Inverting Input, Positive Supply, Negative Supply and Output that correspond to the appropriate pins of the MCP6241 op amp.

The op amp model is self contained and requires no other models or libraries to run. Figure 2 shows how to call the op amp sub circuit from a netlist.

```
.LIB "./mcp6241.lib"
.TRAN  0 100us 0 0.1us
.PROBE V(*) I(*)
R_RG          0 2  10k
R_RL          0 OUT  {RL}
C_CL          0 OUT  {CL}
V_VDD          3 0 {VDD}
V_VSS          0 4 {VDD}
V_VIN          IN 0
+PULSE -2.25 2.25 10u 1p 1p 50u 100u
R_RP          IN 1  10k
R_RF          2 5  {RF}
R_RZ          5 OUT  1m
XOPA 1 2 3 4 5 MCP6241
.PARAM  VDD=2.5 RF=1 CL=60p RL=10k
.END
```

FIGURE 2: *Calling Op Amp Sub Circuit From Main Circuit Netlist.*

In the above netlist, "XOPA" is the call statement for the op amp model MCP6241. The statement .LIB "./ mcp6241.LIB" calls out a file "MCP6241.LIB" which contains the MCP6241 netlist. No other library of parts are required.

SIMULATOR COMPATIBILITY

The original SPICE code, also known as "Berkeley SPICE", was written by the University of California at Berkeley. There are many other SPICE simulators, which have taken this code by Berkeley and modified to their own use. They have either modified the syntax structure, usually allowing more features, and/or modified the convergence algorithm to speed up the simulation and improve convergence. Out of all these simulators, PSPICE by Cadence is one of the most widely accepted general purpose circuit simulators and many SPICE vendors have included options to be "PSPICE compatible". However being compatible does not remove the possibility of syntax errors or convergence issues existing between SPICE and PSPICE simulators.

It was found that in most cases these "PSPICE compatible" simulators could not fully read in a PSPICE netlist without a syntax error. Worst case is when the simulators read in a PSPICE netlist and run it with no error but the results are not correct. This is due to one of the commands not being interpreted correctly and therefore the simulator gives false results. The following are issues that have been seen with so called "PSPICE compatible" simulators:

- Not being able to recognize TABLE syntax
- Limited by the number of TABLE commands
- Not being able to recognize math formula syntax
- Not being able to recognize TCE syntax for resistors
- Commands such as TCE are accepted but does not function and gives no error
- PSPICE adds a resistor to every node to ground but most simulators do not have this feature resulting in convergence issues or different behavior
- MOSFET levels above 3 are not equivalent
- Convergence controls such as tolerance and maximum/minimum step size not the equivalent

CONVERGENCE ISSUES

For most simple circuits with short circuit simulation times, the default settings are sufficient as shown in Figure 3.

Complex circuits that have large voltages, currents, or long circuit simulation time, may result in convergence issues. These convergence issues could be caused by the op amp model, the external circuitry, or the simulators' default convergence parameters. Typically the default convergence parameters for PSPICE are set for certain types of circuits. The following are some helpful hints in fixing these convergence problems if encountered.

First change the following parameters. These do not hurt convergence and can only help.

- Increase the ITL1, ITL2, and ITL4 parameters to 1000. This allows the simulator to try smaller steps allowing for a better chance at converging
- Check the "Use GMIN stepping to improve convergence" option if it is available. This will vary the GMIN parameter which is inversely proportional to the resistance the simulator adds to each node

If the convergence is still an issue, RELTOL, VNTOL, ABSTOL, and CHGTOL parameters can be changed. However, adjusting these parameters can either help or hurt the convergence. It is recommended that the following steps be tried one at a time. If the adjustment does not fix the convergence issue, set it back to the default setting before changing the other parameters.

- Increase the RELTOL parameter to 0.01. This increases the dynamic range of the step size. It is required for circuits that are switching in nanoseconds yet the simulation time is microseconds or higher. This will help the simulator take smaller steps when needed. Going above 0.1 will cause the solutions to be unstable and erroneous results given
- Increase the tolerance parameters such as VNTOL, ABSTOL, and CHGTOL by a factor of 10x with a maximum factor of 100x. For better convergence, increase all of the parameters by the same amount. These parameters set the tolerance on the simulator for solving equations. As an example, in IC's the current can be in µA, but if simulating a switching power supply the currents can be in amps and trying to resolve the currents that are less than 1 µA makes it quite difficult for the simulator
- Configure the simulator to skip the bias point calculation or do not use the initial conditions. Sometimes forcing a condition can cause the simulator to not find the correct solution for the whole circuit
- Adjust the maximum step size to a smaller value. This will force the simulator to take smaller steps, but it may take significantly longer to run.

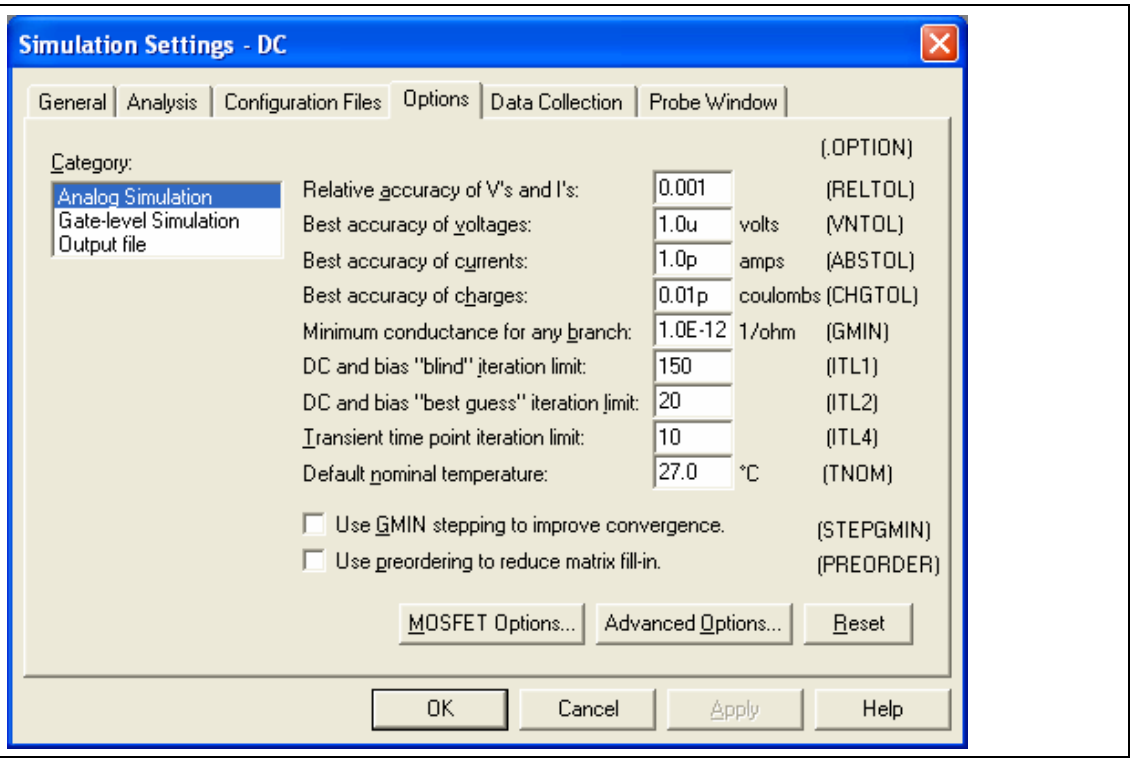

FIGURE 3: *Default PSPICE Settings.*

Convergence between different simulators is always an issue. Each simulator's "claim to fame" is that it can converge better and quicker than the other. They may have better convergence but it is usually on specific types of circuits so it may or may not be better with the op amp model. For example, one simulator may work well with switching power supply circuits that are simplified but not detailed models of linear circuits. The best way to resolve this issue is to compare the different settings for the options such as RELTOL, VNTOL and so forth. In some cases, not all the convergence controls are accessible. In cases such as this, you may need to place small capacitors (1-10 pF), across GTABLES set up as ideal diodes or current limits and actual diode models. If available, you can try the CSHUNT command which adds a capacitor from each node to ground in the circuit. Do not exceed 10 pF because it may start to effect the op amp model characteristics.

One issue to watch for is the GMIN parameter with PSPICE and some other simulators. The input resistances on some of the models are as high as $20 \times 10^{12}\Omega$. This equates to a conductance as low as 5×10^{-14} mhos. The default GMIN setting is 1×10^{-12} mhos, which is like putting a $1 \times 10^{12}\Omega$ resistor on every node to ground. This will decrease the input resistance and effect currents and impedance measurements. If the simulation circuit relies on the input impedances being as high as $20 \times 10^{12}\Omega$, then it is recommended setting GMIN to a conductance less than 5×10^{-16} mhos so it will only effect the simulation by 1%. Designers may also need to tighten the relative tolerances to improve accuracy. If GMIN is not available in the simulator, then most likely it does not add a resistor to ground at every node and this will not affect the input impedance.

PRACTICAL EXAMPLE

The following examples show various application circuits where the op amp models can be used. These examples give an idea on how to test some of the op amp parameters and how to set up the simulator. All examples are based on MCP6241 model and use the default **Options** control shown in Figure 3.

Large Signal Response

The following is an example of a large signal response of the op amp. A pulse is applied to the input and the output is examined.

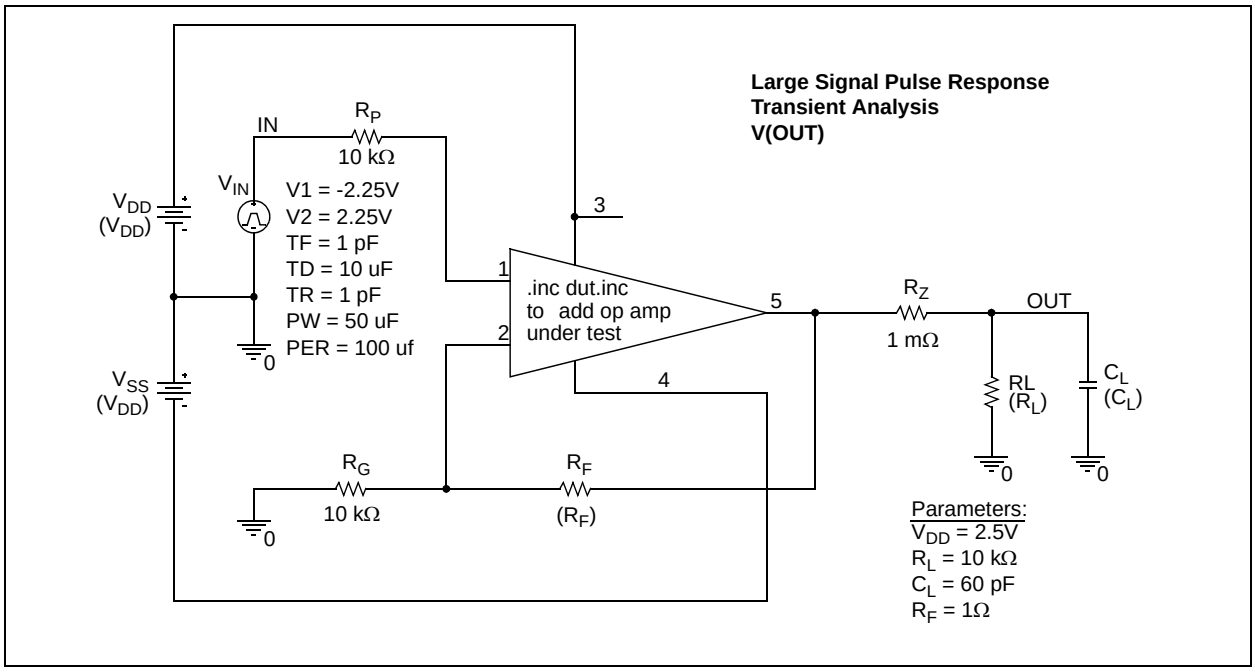

FIGURE 4: *Large Signal Response Circuit.*

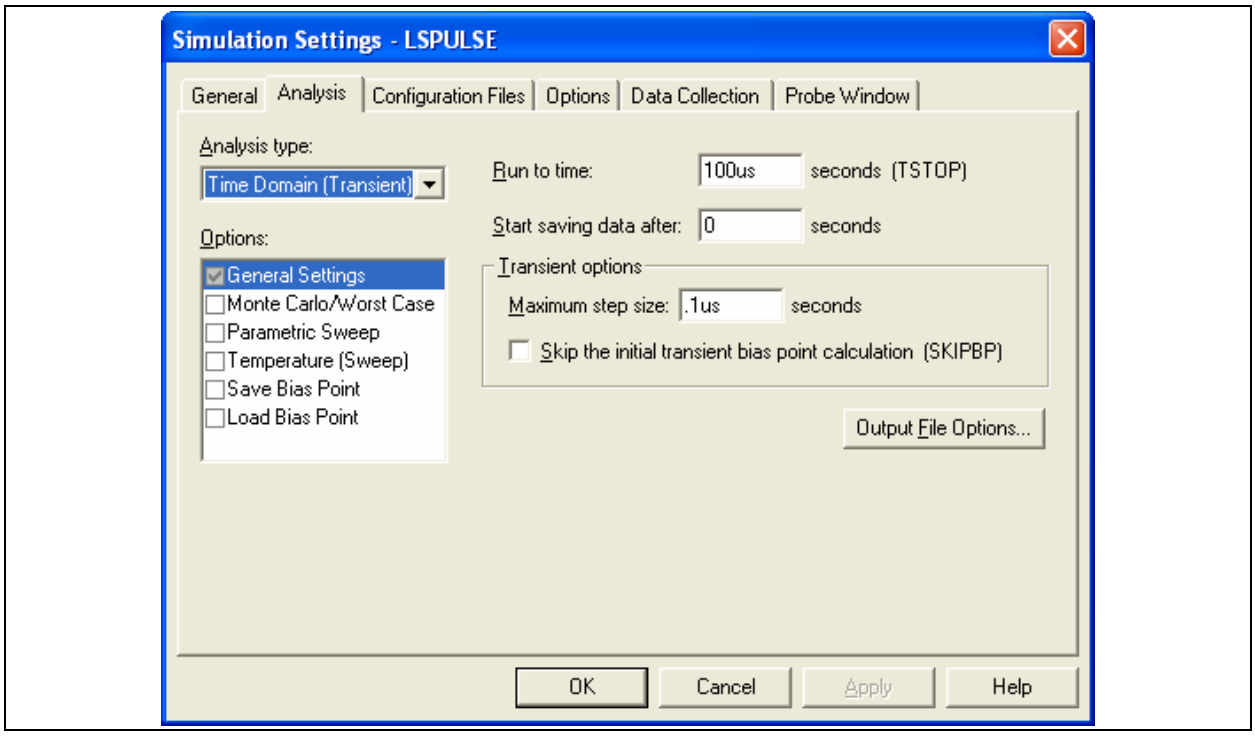

FIGURE 5: *Large Signal Simulation Settings.*

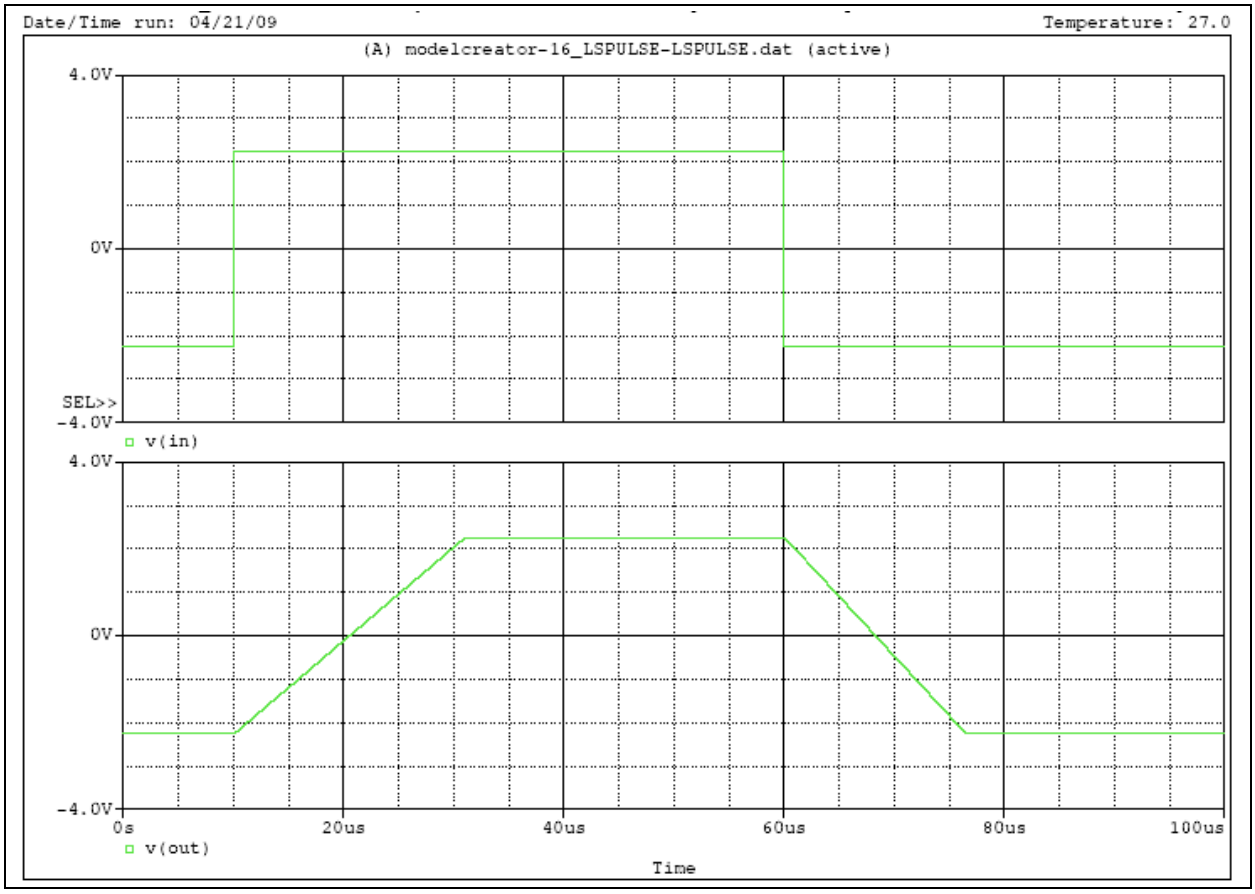

FIGURE 6: *Large Signal Response Waveforms.*

Small Signal Response

The following is an example of a small signal AC response of the op amp. An AC voltage source is applied to the input and output is examined.

The figures below show how to perform a small signal AC analysis on the circuit.

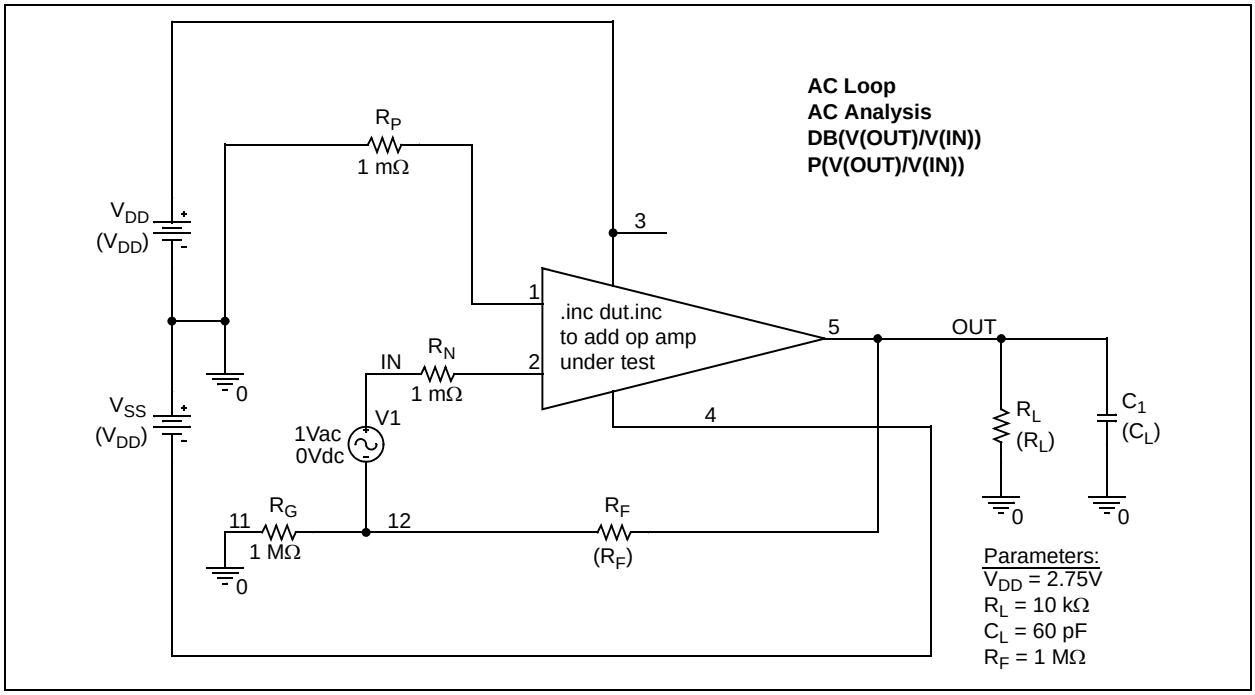

FIGURE 7: *Small Signal AC Response Circuit.*

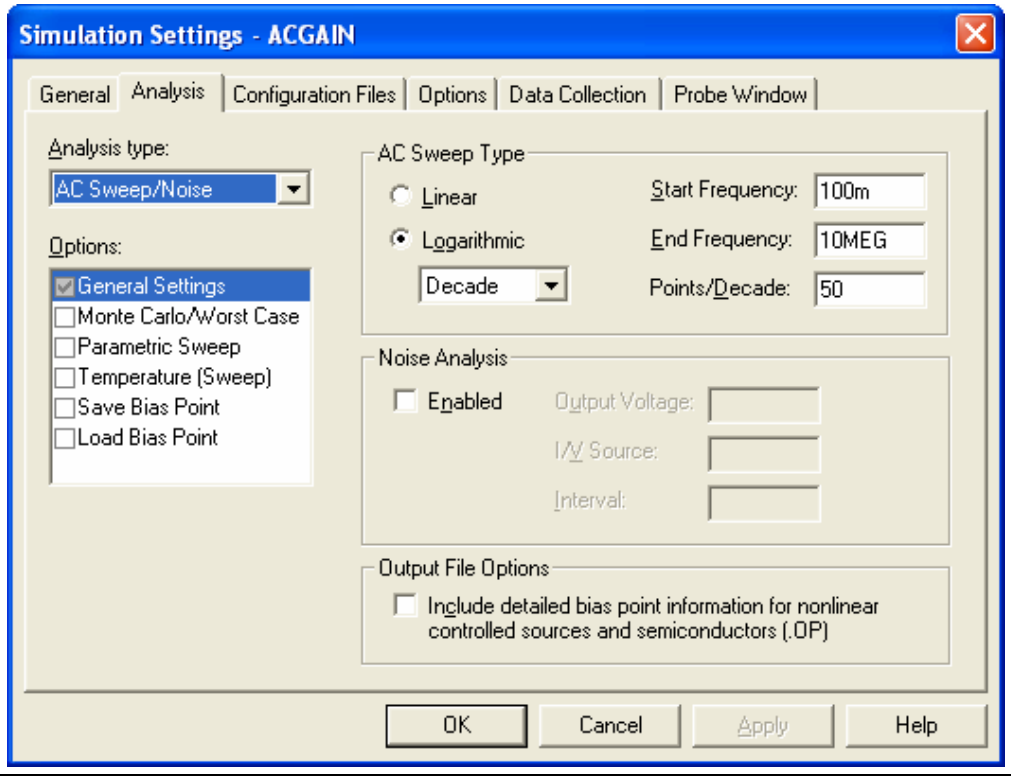

FIGURE 8: *Small Signal AC Simulation Settings.*

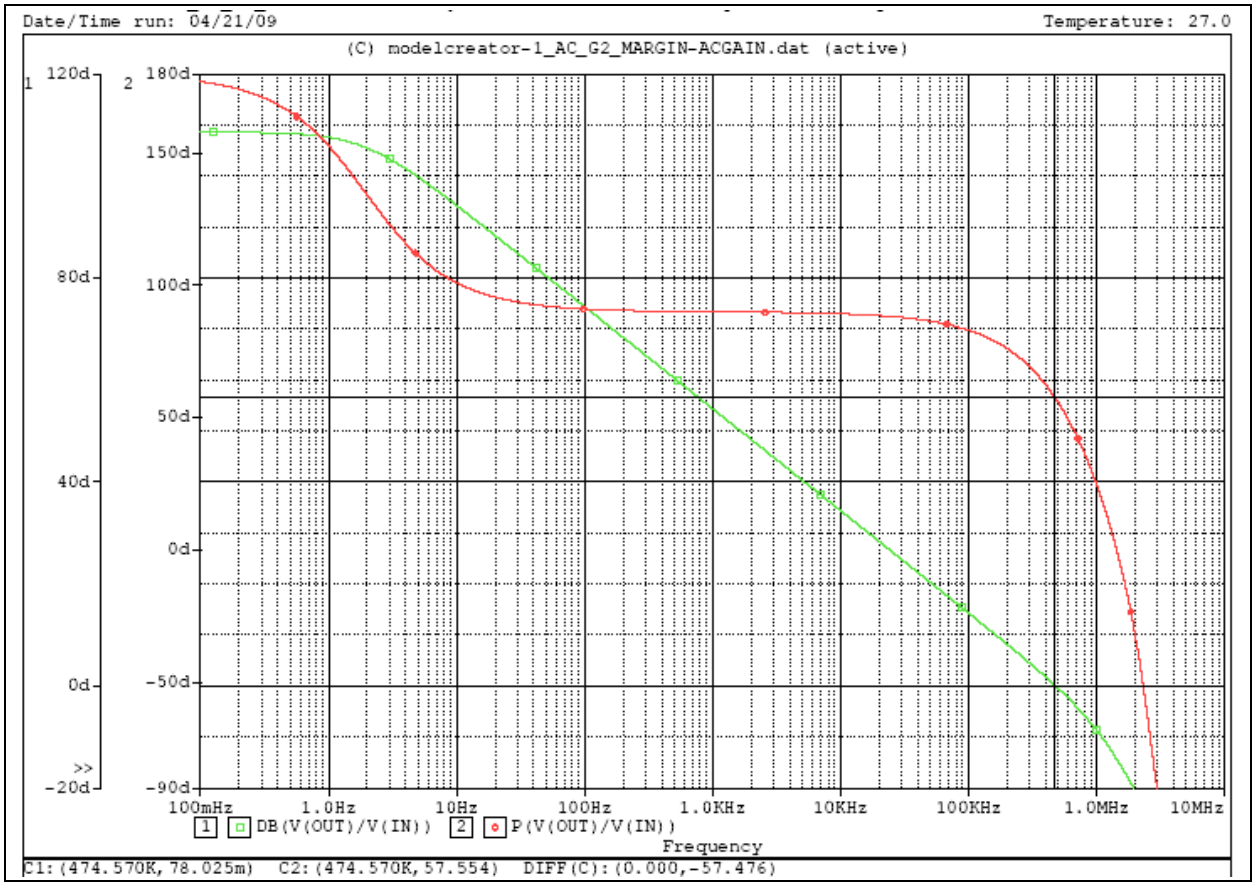

FIGURE 9: *Small Signal AC Response Waveforms.*

Output Short Circuit Current vs. Power Supply Voltage

The following is an example of output short circuit current as a function of V_{DD}, the supply voltage.

This was done at -40°C, +25°C, +85°C and +125°C. The figures below show how to perform sweeps with voltage and temperature on the circuit.

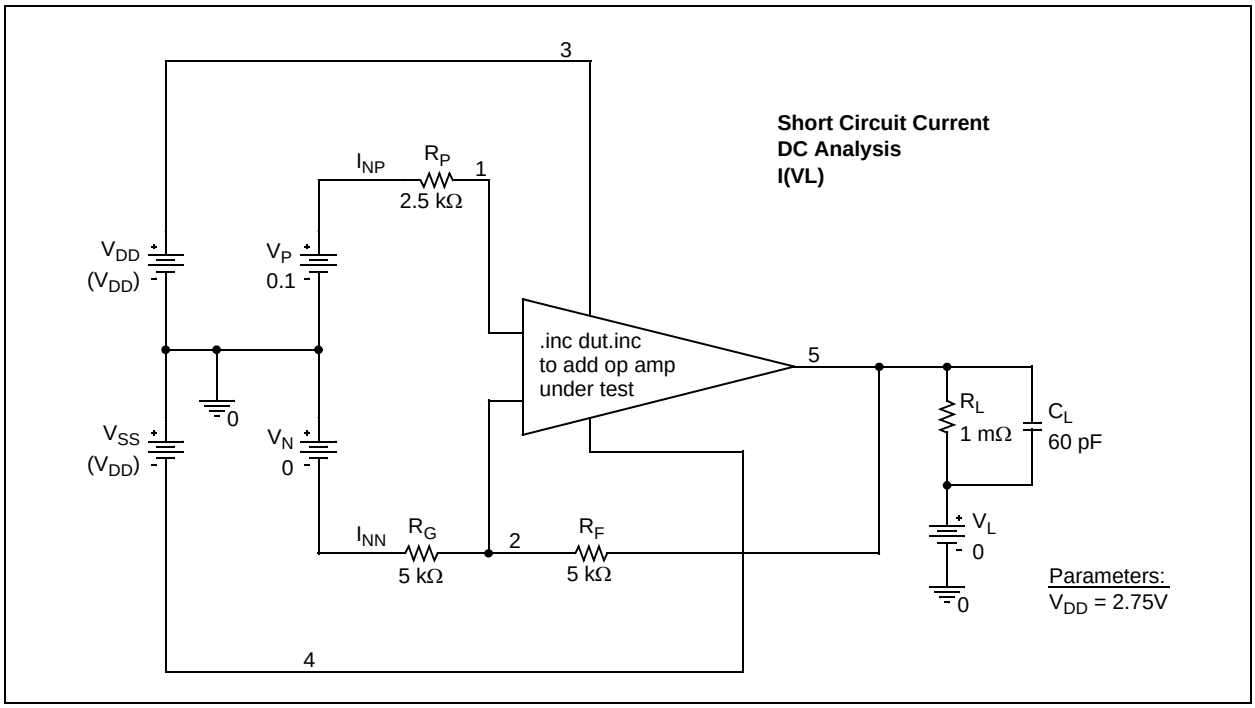

FIGURE 10: *Output Short Circuit Current Circuit.*

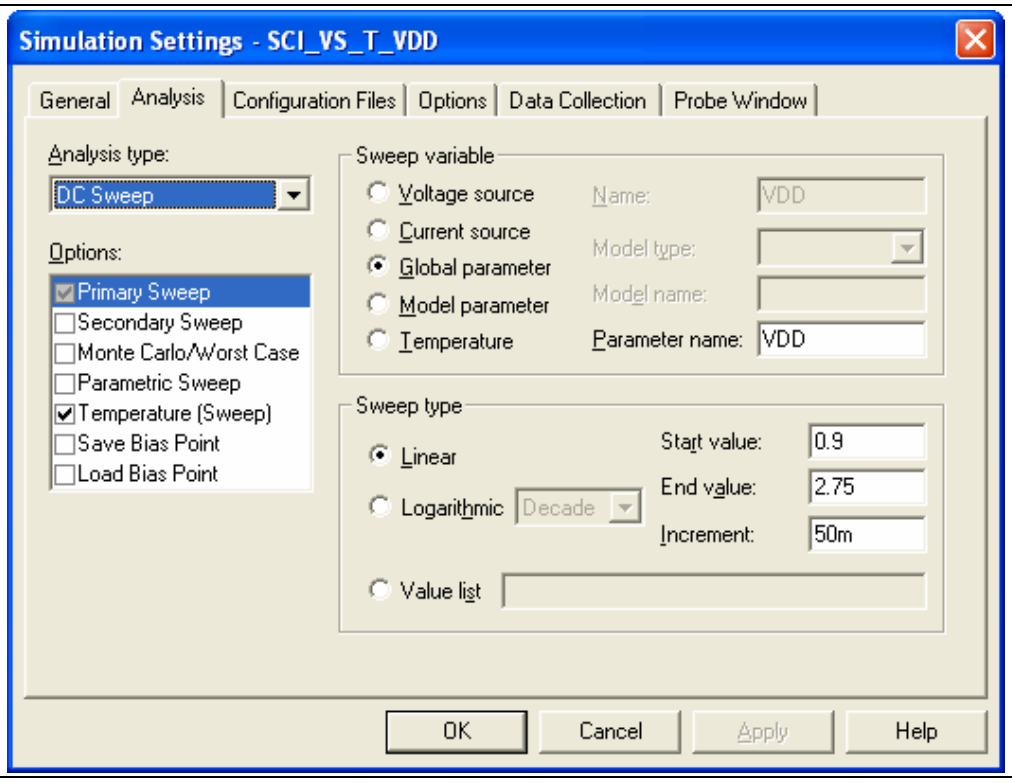

FIGURE 11: *Output Short Circuit Current Simulation Primary Sweep Settings.*

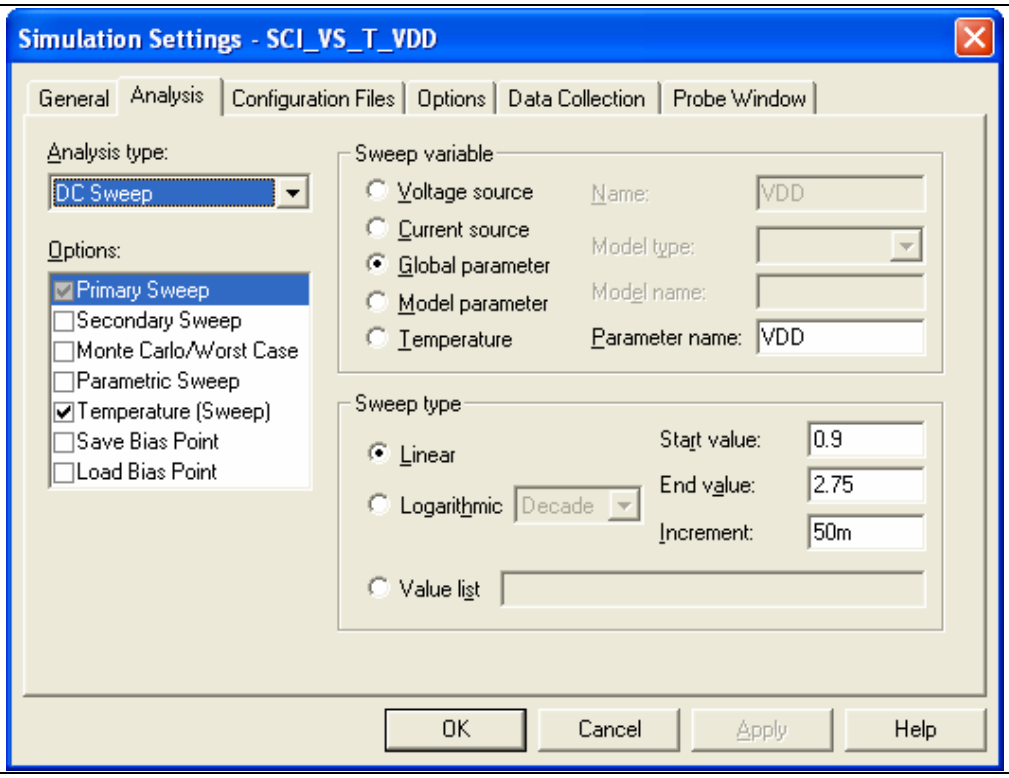

FIGURE 12: *Output Short Circuit Current Simulation Temperature Sweep Settings.*

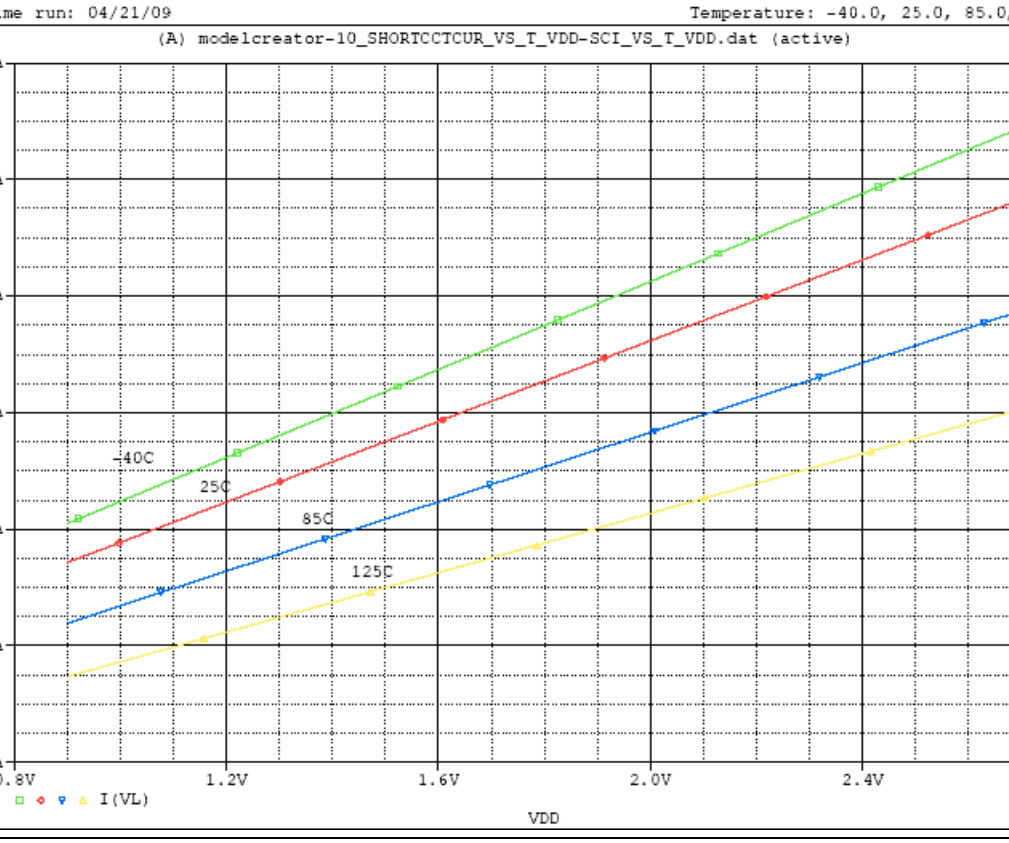

FIGURE 13: *Output Short Circuit Current vs. Power Supply Voltage Waveforms.*

Input Noise Voltage Density vs. Frequency

The following is an example of the noise generated from the op amp as a function of frequency.

This was done at -40°C, +27°C and +125°C. The figures below show how to perform a Noise analysis on the circuit.

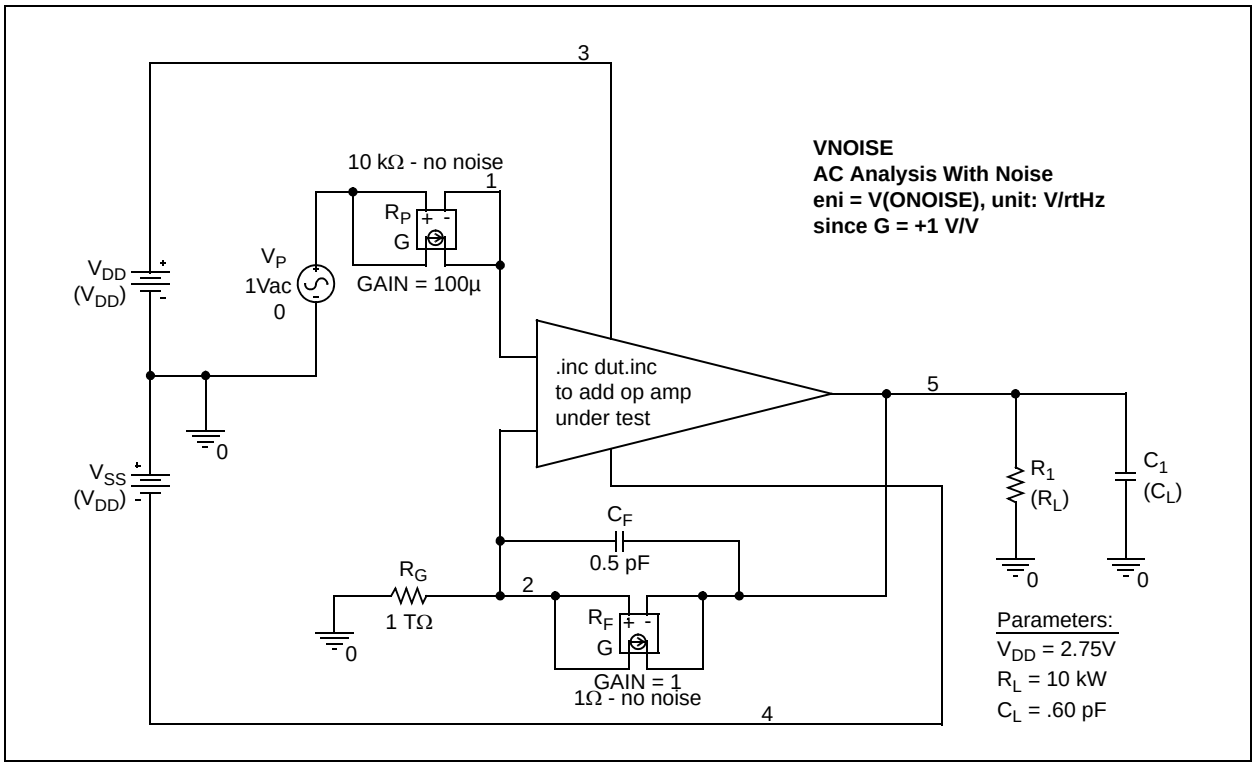

FIGURE 14: *Noise Voltage Density Circuit.*

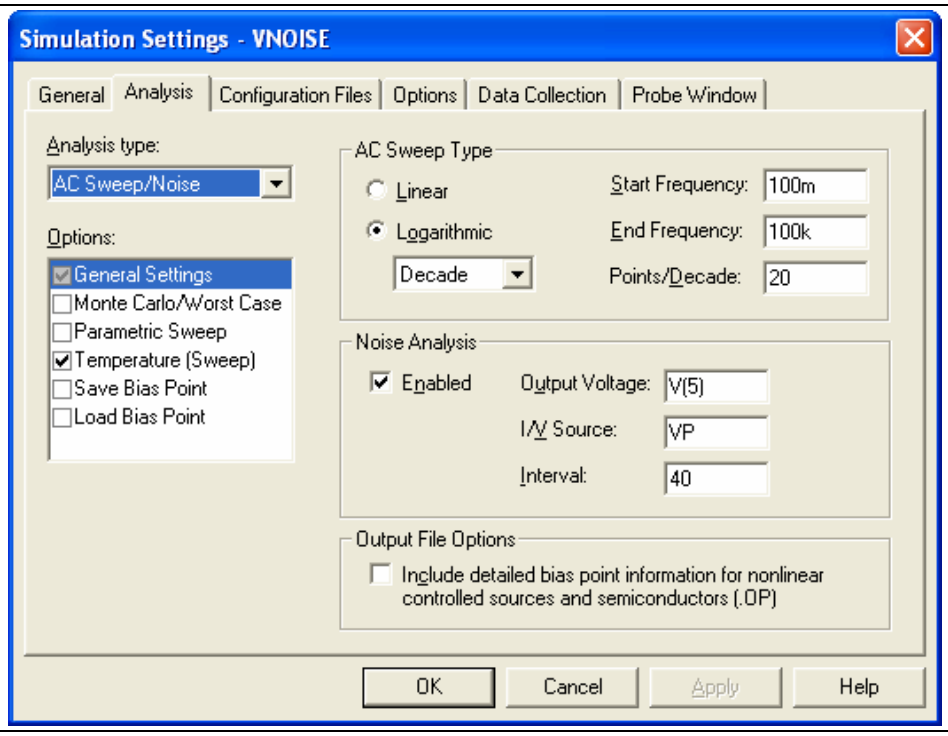

FIGURE 15: *Noise AC Sweep Settings.*

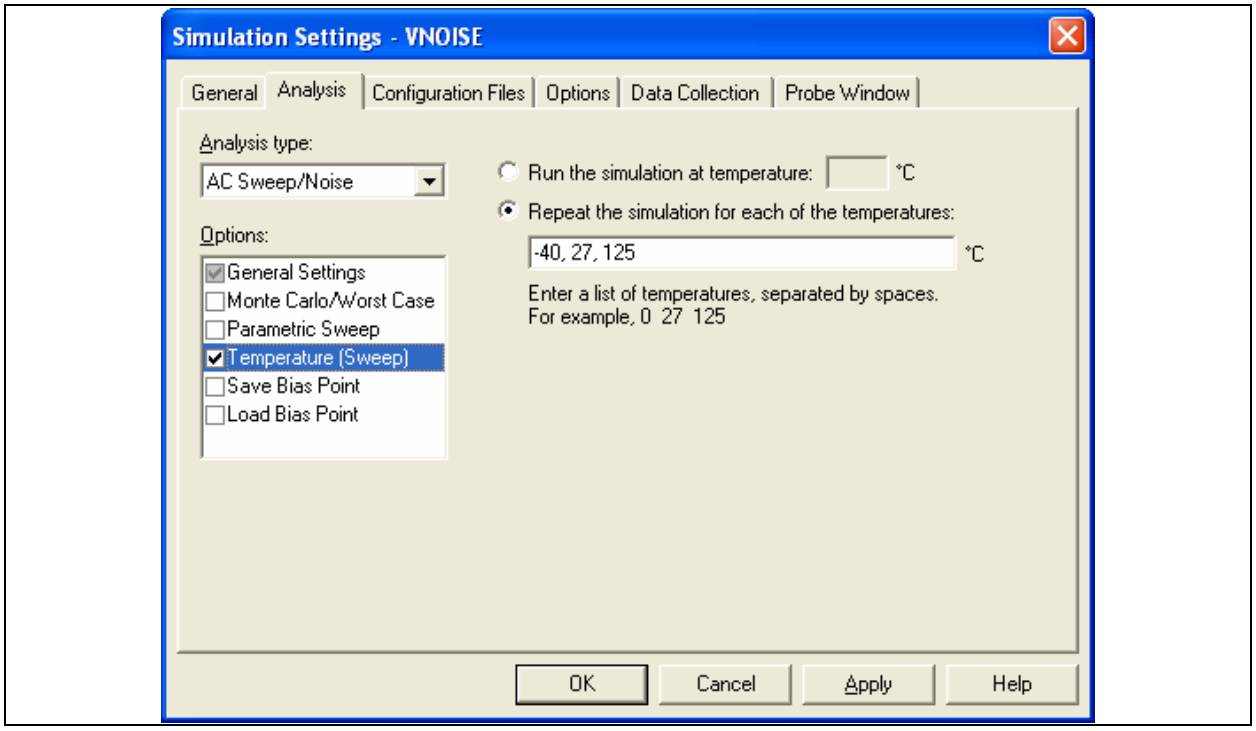

FIGURE 16: *Noise Temperature Sweep Settings.*

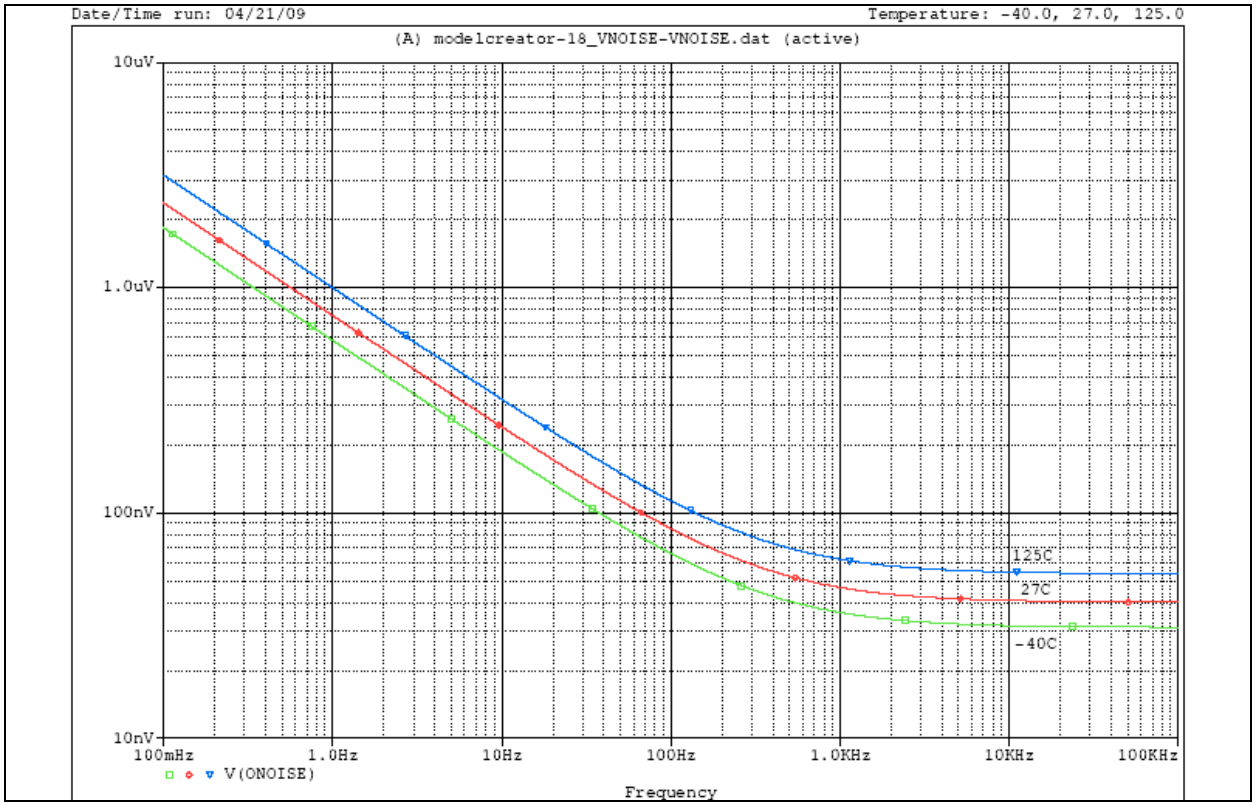

FIGURE 17: *Input Noise Voltage Density vs. Frequency Waveforms*

The complete SPICE macro models netlist for the simulated MCP6241 in the practical example can be found in **Appendix A: "MCP6241 SPICE Macro Model Netlist"**.

APPENDIX A: MCP6241 SPICE MACRO MODEL NETLIST

```
.SUBCKT MCP6241 1 2 3 4 5
*               | | | | |
*               | | | | Output
*               | | | Negative Supply
*               | | Positive Supply
*               | Inverting Input
*               Non-inverting Input
*
********************************************************************************
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********************************************************************************
*
* The following op-amps are covered by this model:
*      MCP6241,MCP6242,MCP6244
*
* Revision History:
*      REV A: 21-Aug-06, Created model
*      REV B: 27-Jul-07, Updated output impedance for better model stability w/cap load
*
* Recommendations:
*      Use PSPICE (other simulators may require translation)
*      For a quick, effective design, use a combination of: data sheet
*            specs, bench testing, and simulations with this macromodel
*      For high impedance circuits, set GMIN=100F in the .OPTIONS statement
*
* Supported:
*      Typical performance for temperature range (-40 to 125) degrees Celsius
*      DC, AC, Transient, and Noise analyses.
*      Most specs, including: offsets, DC PSRR, DC CMRR, input impedance,
*            open loop gain, voltage ranges, supply current, ... , etc.
*      Temperature effects for Ibias, Iquiescent, Iout short circuit
*            current, Vsat on both rails, Slew Rate vs. Temp and P.S.
*
* Not Supported:
*      Some Variation in specs vs. Power Supply Voltage
*      Monte Carlo (Vos, Ib), Process variation
*      Distortion (detailed non-linear behavior)
*      Behavior outside normal operating region
```

```
*
* Input Stage
V10  3 10 -500M
R10 10 11 6.90K
R11 10 12 6.90K
C11 11 12 7.20P
C12  1  0 6.00P
E12 71 14 POLY(4) 20 0 21 0 26 0 27 0   5.00M 34.9 34.9 1 1
G12 1 0 62 0 1m
M12 11 14 15 15 NMI
M14 12 2 15 15 NMI
G14 2 0 62 0 1m
C14  2  0 6.00P
I15 15 4 50.0U
V16 16 4 -300M
GD16 16 1 TABLE {V(16,1)} ((-100,-1p)(0,0)(1m,1u)(2m,1m))
V13 3 13 -300M
GD13 2 13 TABLE {V(2,13)} ((-100,-1p)(0,0)(1m,1u)(2m,1m))
R71  1  0 20.0E12
R72  2  0 20.0E12
R73  1  2 20.0E12
I80  1  2 500E-15
*
* Noise, PSRR, and CMRR
I20 21 20 423U
D20 20  0 DN1
D21  0 21 DN1
G26  0 26 POLY(2) 3 0 4 0   0.00 -158U -3U
R26 26  0 1
G27  0 27 POLY(2) 1 0 2 0  -776U 35.5U 35.5U
R27 27  0 1
*
* Open Loop Gain, Slew Rate
G30  0 30 12 11 1
R30 30  0 1.00K
C30 30 0 10p
G31 0 31 3 4 2
I31 0 31 DC 65
R31 31  0 1 TC=3.67M,5.32U
GD31 30 0 TABLE {V(30,31)} ((-100,-1u)(0,0)(1m,.1)(2m,2))
G32 32 0 3 4 -1.9
I32 32 0 DC 105
R32 32  0 1 TC=3.43M,4.42U
GD32 0 30 TABLE {V(30,32)} ((-2m,2)(-1m,.1)(0,0)(100,1u))
G33  0 33 30 0 1m
R33  33 0 1K
G34  0 34 33 0 316M
R34  34 0 1K
C34  34 0 81.8U
G37  0 37 34 0 1m
R37  37 0 1K
C37  37 0 22.7P
G38  0 38 37 0 1m
R38  39 0 1K
L38  38 39 26.5U
E38  35 0 38 0 1
G35 33 0 TABLE {V(35,3)} ((-1,-1n)(0,0)(48,1n))(49,1))
G36 33 0 TABLE {V(35,4)} ((-49,-1)((-48,-1n)(0,0)(1,1n))
*
* Output Stage
R80 50 0 100MEG
G50 0 50 57 96 2
R58 57  96 0.50
R57 57  0 1650
C58  5  0 2.00P
G57  0 57 POLY(3) 3 0 4 0 35 0   0 0.21M 0.21M 0.6M
GD55 55 57 TABLE {V(55,57)} ((-2m,-1)(-1m,-1m)(0,0)(10,1n))
GD56 57 56 TABLE {V(57,56)} ((-2m,-1)(-1m,-1m)(0,0)(10,1n))
E55 55  0 POLY(2) 3 0 51 0 -0.85M 1 -51.0M
E56 56  0 POLY(2) 4 0 52 0 1.33M 1 -42.0M
R51 51 0 1k
R52 52 0 1k
```

```
GD51 50 51 TABLE {V(50,51)} ((-10,-1n)(0,0)(1m,1m)(2m,1))
GD52 50 52 TABLE {V(50,52)}  ((-2m,-1)(-1m,-1m)(0,0)(10,1n))
G53  3  0 POLY(1) 51 0  -50.0U 1M
G54  0  4 POLY(1) 52 0  -50.0U -1M
*
* Current Limit
G99 96 5 99 0 1
R98 0 98 1 TC=-1.92M,-7.58U
G97 0 98 TABLE { V(96,5) } ((-11.0,-21.0M)(-1.00M,-20.7M)(0,0)(1.00M,20.7M)(11.0,21.0M))
E97 99 0 VALUE { V(98)*((V(3)-V(4))*166M + 416M)}
D98 4 5 DESD
D99 5 3 DESD
*
* Temperature / Voltage Sensitive IQuiscent
R61 0 61 1 TC=3.14M,7.28U
G61 3 4 61 0 1
G60 0 61 TABLE {V(3, 4)}
+ ((0,0)(750M,450N)(800M,1.00U)(900M,4.00U)
+ (1.2,41.0U)(1.4,45.0U)(5.5,46.0U))
*
* Temperature Sensistive offset voltage
I73 0 70 DC 1uA
R74 0 70 1 TC=3.00U
E75 1 71 70 0 1
*
* Temp Sensistive IBias
I62 0 62 DC 1uA
R62 0 62 REXP 55.78U
*
* Models
.MODEL NMI NMOS(L=2.00U W=42.0U KP=20.0U LEVEL=1 )
.MODEL DESD  D   N=1 IS=1.00E-15
.MODEL DN1 D   IS=1P KF=146E-18 AF=1
.MODEL REXP RES TCE=10.14
.ENDS MCP6241
```

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Fax: 972-818-2924

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Fax: 248-538-2260

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Tel: 765-864-8360
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Fax: 408-961-6445

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Mississauga, Ontario,
Canada
Tel: 905-673-0699
Fax: 905-673-6509

ASIA/PACIFIC

Asia Pacific Office
Suites 3707-14, 37th Floor
Tower 6, The Gateway
Harbour City, Kowloon
Hong Kong
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Fax: 852-2401-3431

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Fax: 66-2-694-1350

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Fax: 34-91-708-08-91

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Fax: 44-118-921-5820

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